IN THE CLAIMS:

Please amend the claims to read in full as follows:

1   1. (Amended) A method of eliminating parasitic bipolar transistor action in a Silicon on
2   Insulator (SOI) Metal Oxide Semiconductor (MOS) device located in a logic circuit, said logic
3   circuit being adapted to receive an input signal and a clock signal, the method comprising:
4   controlling the conduction of an active discharging device with the input signal, said
5   active discharging device being coupled to an intermediate node of said logic circuit,
6   whereby the parasitic bipolar transistor is deactivated.

1   2. (Amended) The method of claim 1, wherein the SOI device comprises a gate and a
2   drain, and wherein the method further comprises:
3   providing a first signal to said gate of said SOI device;
4   providing a second signal to said drain of said SOI device; and
5   activating the conduction of said active discharging device according to the state of said
6   first signal.

1   3. (Amended) The method of claim 2 wherein the first signal is said input signal.

1   4. (Amended) The method of claim 2 wherein said first signal causes said SOI device to
2   conduct current whenever said logic circuit is being pre-charged.

1   5. (Amended) The method of claim 2 wherein the second signal pre-charges said drain
2   during a pre-charge cycle.

1   6. (Amended) The method according to claim 1, wherein the active discharging device
2   provides a conduction path between said intermediate node and a voltage source.

Docket No.: RO998-200B   2
Serial No.: 09/334,171

1   7. (Amended) A method of eliminating parasitic bipolar transistor action in a Silicon on

2 Insulator (SOI) Metal Oxide Semiconductor (MOS) dynamic logic circuit having an input, an

3 output, a clock, an active discharge transistor, and a plurality of stacked SOI Metal Oxide

4 Semiconductor (MOS) transistors interconnected to define a common node and an intermediate

5 node, wherein:

6   said plurality of stacked SOI MOS transistors is controlled by a plurality of inputs;

7   said common node is coupled to a pre-charging device;

8   said intermediate node is in a path between said common node and a voltage source, said

9   path defined by said plurality of stacked SOI MOS transistors;

10   said intermediate node is coupled to said common node by at least a first of said plurality

11   of stacked SOI MOS transistors; and

12   said active discharging transistor is controlled by at least one of said plurality of inputs,

13   said active discharging transistor defining a discharge path between said intermediate

14   node and said voltage source,

15 the method comprising:

16   controlling the conduction of said active discharging transistor during a pre-charge cycle;

17 and

18   actively discharging said intermediate node, whereby the parasitic bipolar transistors are

19 deactivated and the charge at said intermediate node is maintained at a predetermined level.

1   8. (Unchanged) The method according to claim 7, wherein pre-charging occurs during a

2 low state of said clock.

1   9. (Unchanged) The method according to claim 7, wherein pre-charging occurs during a

2 high state of said clock.

1   10. (Unchanged) The method according to claim 7, wherein during the pre-charging all

2 said inputs are set to a predetermined logic state.

1   11. (Unchanged) The method according to claim 10, wherein said logic state is low.

1   12. (Unchanged) The method according to claim 10, wherein said logic state is high.

1   13. (Unchanged) The method according to claim 7, wherein the step of actively

2   discharging said intermediate nodes prevents the body voltages of said stacked SOI transistors

3   from reaching a voltage stage sufficient to activate the parasitic bipolar transistors of said stacked

4   SOI transistors.

1   14. (Unchanged) The method according to claim 7, wherein said stacked transistors are

2   N-Field Effect Transistors (NFET) and said active discharging transistors are P-Field Effect

3   Transistors (PFET).

1   15. (Unchanged) The method according to claim 7, wherein said stacked transistors are

2   P-Field Effect Transistors (PFET) and said active precharging transistors are N-Field Effect

3   Transistors (NFET).

1   16. (Unchanged) The method according to claim 7, wherein said pre-charging device

2   comprises transistors coupled to said stacked transistors.

Please add the following new claims:

1   17. (New) A method of reducing the effects of parasitic bipolar transistor action in a

2   silicon-on-insulator (SOI) logic circuit during a pre-charge cycle, comprising:

3   coupling an active discharge device to an intermediate node of the SOI logic circuit; and

4   controlling the conduction of the active discharging device using a non-clock signal,

5   whereby the charge at the intermediate node is maintained at a predetermined level during the

6   pre-charge cycle.

1   18. (New) The method of claim 17, wherein the predetermined level is a common ground

2   potential for the SOI logic circuit.

1   19. (New) The method of claim 17, wherein the non-clock signal comprises an active

2   low signal applied to an input of the SOI logic circuit during the pre-charge cycle.

1   20. (New) The method of claim 1, wherein said input signal is a non-clock signal.

1   21. (New) The method of claim 6, wherein the voltage source comprises a system

2   ground.